HIGH RELIABILITY, HIGH MIX, ULTRALOW VOLUME SURFACE MOUNT TECHNOLOGY FOR SPACE APPLICATIONS

by

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AIMTRACT

For the past two years, the Jet Propulsion Laboratory (JPL) in Pasadena, California has been working to introduce surface mount technology (SMT) for high reliability space applications. This thrust has centered around four research and development projects, the aim of which is to facilitate the use of SMT for designing, producing, inspecting, and qualifying surface mount printed wiring assemblies for ultralow volume, long life space applications. Although the older planar mount technology proved to be useful for such applications, the development of greater pin count for active devices coupled with finer features on the printed wiring board has pushed advanced electronics towards the use of SMT to meet the ever increasing demands of spacecraft (S/C) technology. Nevertheless, the special requirements of spacecraft, such as the extreme high reliability requirement along with very low production runs, have necessitated carefully tailoring SMT to meet these stringent demands. In particular, SMT for S/C can be characterized as ultralow volume concomitant with the need for very high reliability. This paper explores the current approach being pursued at JPL and some of the problems peculiar to applying SMT to S/C application.

INTRODUCTION

S/C applications impose several unique issues. First, the ultrasmall production quantity strongly affects the strategy and practices in the fabrication and assembly processes, inspection, and qualification, Diversified mission-specific operating environments can range from shuttle missions of a few days duration to multiyear service life (10 years or more) required for deep space missions to the far reaches of the solar system. Because there is usually minima] feedback from field operations and because repair of faulty components is often very difficult, if not impossible, assessments of component and interconnect integrity have to rely heavily on analytical predictions and qualification testing based on accelerated environments.

There are four research and development efforts presently being pursued at JPL to integrate SMT into spacecraft technology. Each of these efforts deals with one aspect of SMT. In addition, they are all interdependent and are being conducted concurrently. The chief formal mechanism whereby concurrence is being effected is the JPL SMT RTOP Working Group. This group meets on the average of once a week; the emphasis has been on good communication among the differ-

ent participants and personnel. The continuous exchange of information is vital. The four groups and four areas of concern are:

1 Electronic packaging.

2 Quality assurance and process/hardware qualification.

3 Reliability and test qualification.

4 Modeling.

OBJECTIVES

The four SMT research and development efforts focus on the use of SMT for high reliability, low volume production spacecraft electronics as used in the NASA community. Each effort concentrates its efforts on a particular aspect of the design, manufacturing, test, and deployment (ageing) cycle. These efforts have sponsored a series of tests called the Phase 1, Phase 2, and Phase 3 tests, which are being performed at JPL. The Phase 1,2 and 3 tests are cooperative efforts involving all participants.

The primary objectives of the research and development efforts areas follows:

- Identify the critical parameters of SMT manufacture for ultralow volume applications and determine the methods and tools required to integrate quality assurance procedures into the design and manufacturing processes so that the critical parameters may be bounded and controlled.

- Develop a thorough understanding of the creep-fatigue mechanisms underlying solder joint failures of surface mount electronic packaging systems and develop generic, broadly applicable design guidelines, analysis methodologies, and data requirements.

- Develop an assembly level qualification test methodology for surface mount technology and apply this methodology to electronic packaging systems through the use of experimental design techniques and phased experimentation.

- Deliver the NASA Handbook (NHB) for SMT, developed from the knowledge gained from the JPL research and development efforts, as well as the efforts of other NASA centers, industry knowledge centers (IPC, EMPF, CALCE EPRC, NCMS, RELTECH), and industry partners.

SMT RESEARCH AND DEVELOPMENT ACTIVITIES AT JPL

The principal activities in SMT currently underway at JPL are:

- Phase 1 Test
- The Solder Joint Life Prediction Model (SJLPM) Round Robin Effort
- Phase 2 and Phase 3 Tests
- NASA SMT Handbook
- Solder Integrity
- Quality Assurance Methodology
- Qualification Test Technology
- Interactions and collaborations with academia, industry, professional societies, and other NASA installations.

These various activities are briefly summarized below.

PHASE 1 TEST

Summary of Phase 1 Test

The Phase 1 test involves surface mount components (SMCs) soldered to epoxy-fiberglass FR-4 boards. There is one component per board; all components have ceramic bodies and a 0.050" pitch. The three component styles chosen for the test were:

- Leadless chip carriers (LCCs) having **20,28,** and 68 terminations (LCC20, LCC28, LCC68).
- J-lead Cerquads with 68 leads (J-Cerquad68).
- Gull wing Cerquads having **68** leads (Gull wing Cerquad68).

Although a fair number of the solder joints on the test assemblies would normally be classified as rejects, the test assemblies provide a unique opportunity to investigate the lifetimes of various workmanship defects.

Thermomechanical cycle testing on Phase 1 assemblies having LCCS began in August, 1993. All assemblies were subjected to the NASA NHB 5300.4 (3A-1) standard thermal cycle profile consisting of a four hour duration time from -55°C to +100°C. While the low temperature extreme introduces modeling complexities, a previous goal of a single cycle covering all NASA missions resulted in this temperature range.

All LCC assemblies have failed. Phase 1 testing of the J-Cerquads was initiated in January, 1994, and testing of the gull wing Cerquads began in mid-July, 1994. This latter testing is still ongoing and is expected to be completed in 1995. One hundred percent initial and final inspection was performed on all assemblies tested.

SOLDER JOINT RELIABILITY VALIDATION ROUND ROBIN EFFORT

Objectives of the Round Robin Effort

There are three (3) objectives. These are:

- Assess the variability of different solder joint life prediction models (SJLPMs) for identical solder joint reliability problems.
- Review and compare different approaches with experimental results to establish common calibration points.
- Assess different prediction schemes for their most appropriate application for different failure criteria.

A cogent example of the last would be whereas one particular LPM may be best employed to evaluate early damage signals, e.g., the first appearance of a crack (crack initiation), another LPM may be more suitable for predicting total cycles to failure for 50% of the solder joints.

SJLPMS were exercised by various round robin participants, and a summary of the results was distributed to all participants in early November, 1994 for review and comments. A workshop to discuss results to date, lessons learned, and future progress was held at JPL in December.

Continuation of the Round Robin during Phases 2 and 3

The round robin validation effort will be continued during the Phase 2 and 3 tests (see below). A final report summarizing the finding of the Solder Joint Reliability Validation Round Robin will be issued. Appropriate findings will be incorporated into the NASA Surface Mount Technology Handbook (SMT NHB).

PHASE 2 AND 3 TESTING

Approach and Objectives

The overall approach of the Phase 2/3 testing is to perform statistically significant testing of surface mount assemblies in order to better understand the principal failure modes and inherent fatigue life and the continued development of tailored qualification methods. This understanding is necessary in order to establish appropriate use environments (maximum and minimum temperatures, thermal cycling rate and range, dwell times, etc.) and qualification test programs for various combinations of surface mount components (printed circuit board materials, component types, component lead types, etc.).

The specific statistical approach to be utilized in the Phase 2/3 testing is that of fractional factorial experiments. This method, also called the Taguchi method, allows for the maximum number of variables to be studied using the fewest number of test samples. An examination of the possible variables which could potentially impact the reliability of a surface mount assembly (SMA) yielded far more than could be studied in one experimental program. Even reducing the variables to those which are commonly believed to have the most impact results in an excessively large parameter space, Clearly, an intelligent maximization of the number of variables under study while minimizing the number of test articles must be made. The phased Taguchi approach is advantageous for testing where the relative significance of various parameters is not adequately known, as subsequent testing may be performed to further explore “driver” variables and their interactions.

Phase 2 and 3 testing will consist of flight-like thermal cycling, i.e. thermal cycling within a vacuum environment in addition to the usual atmosphere environmental testing. Not unlike flight projects, significant challenges arise when attempting to make optimum use of qualification test resources, A significant number of different surface mount components and technologies will be tested. To achieve statistically significant results requires testing a significant number of devices

and boards. Correspondingly, there is a need to provide a reasonable level of failure site resolution among the large number of SMT device types and quantities. The interior of the vacuum chamber contains many multiplex circuits which, combined with 4-point resistance measurements, result in the capability of up to 700 separate resistance measurements with greater refinement possible to isolate failure sites further. More detailed descriptions of the experimental variables, the experimental configuration, the test vehicles and circuits, and the test hardware and software is given in the following sections.

Test Vehicle/Circuit

The artwork for the Phase 2/3 test vehicles is shown in Figure 1. The completed assemblies consist of a number of daisy chained components allowing electrical resistance measurements. All chip carriers are ceramic. There are also a numerous passive devices on the test assembly. The types of components found on an individual test assembly are:

- 256 gullwing QFP @ 0.020" pitch
- 164 gullwing QFP @ 0.025" pitch
- 68 LCC and 28 LCC @ 0.050" pitch
- 68 J-lead and 28 J-1ead carrier @ 0,050" pitch.

The test assembly contains three primary measurement circuits:

- Daisy-chained resistance (for chip carrier packages)
- LC response (for inductors and small value capacitors)
- RC response (for resistors and larger value capacitors),

The functional test board layout is shown in Figure 2.

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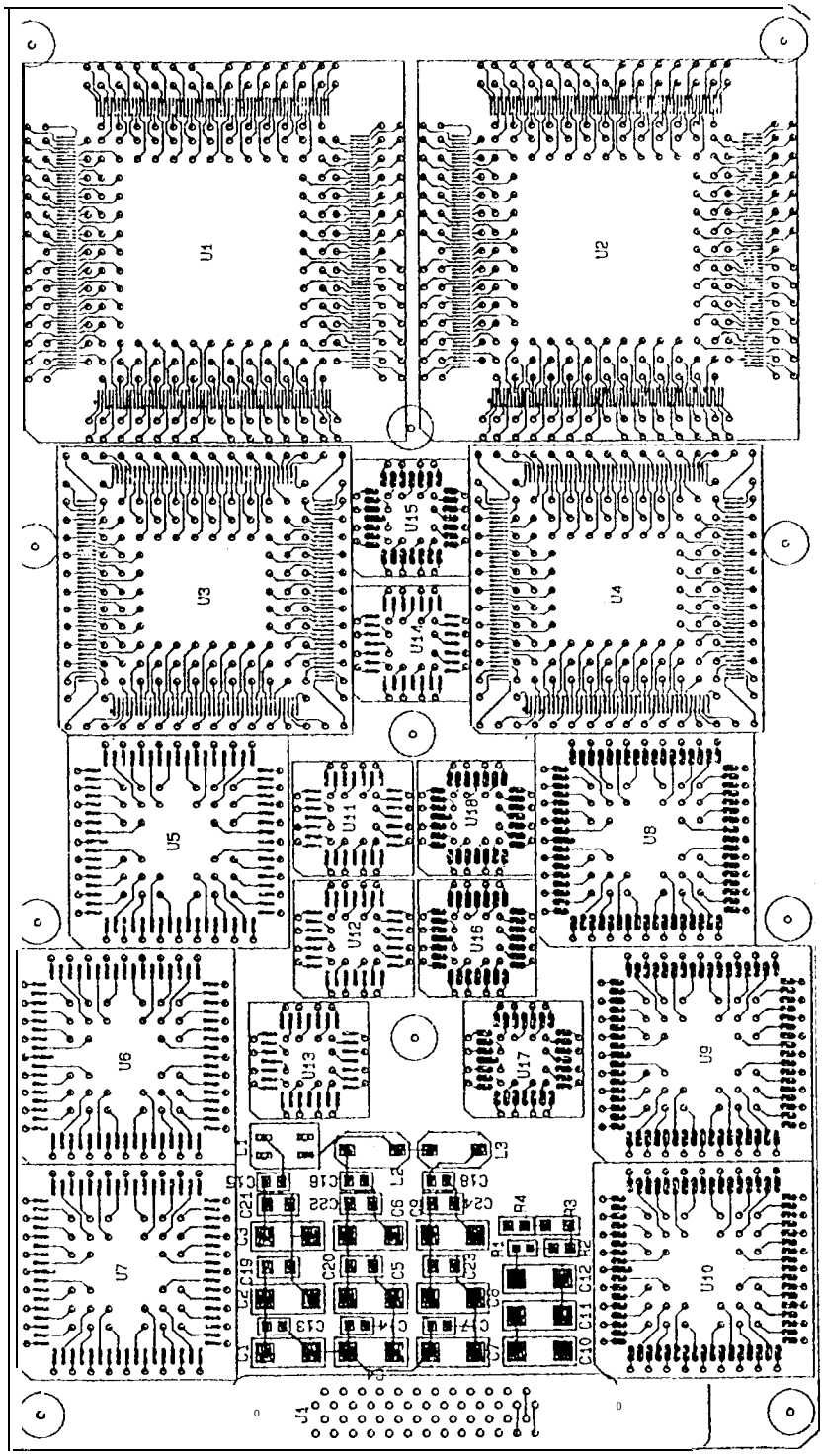

Figure 1 Artwok for the test board

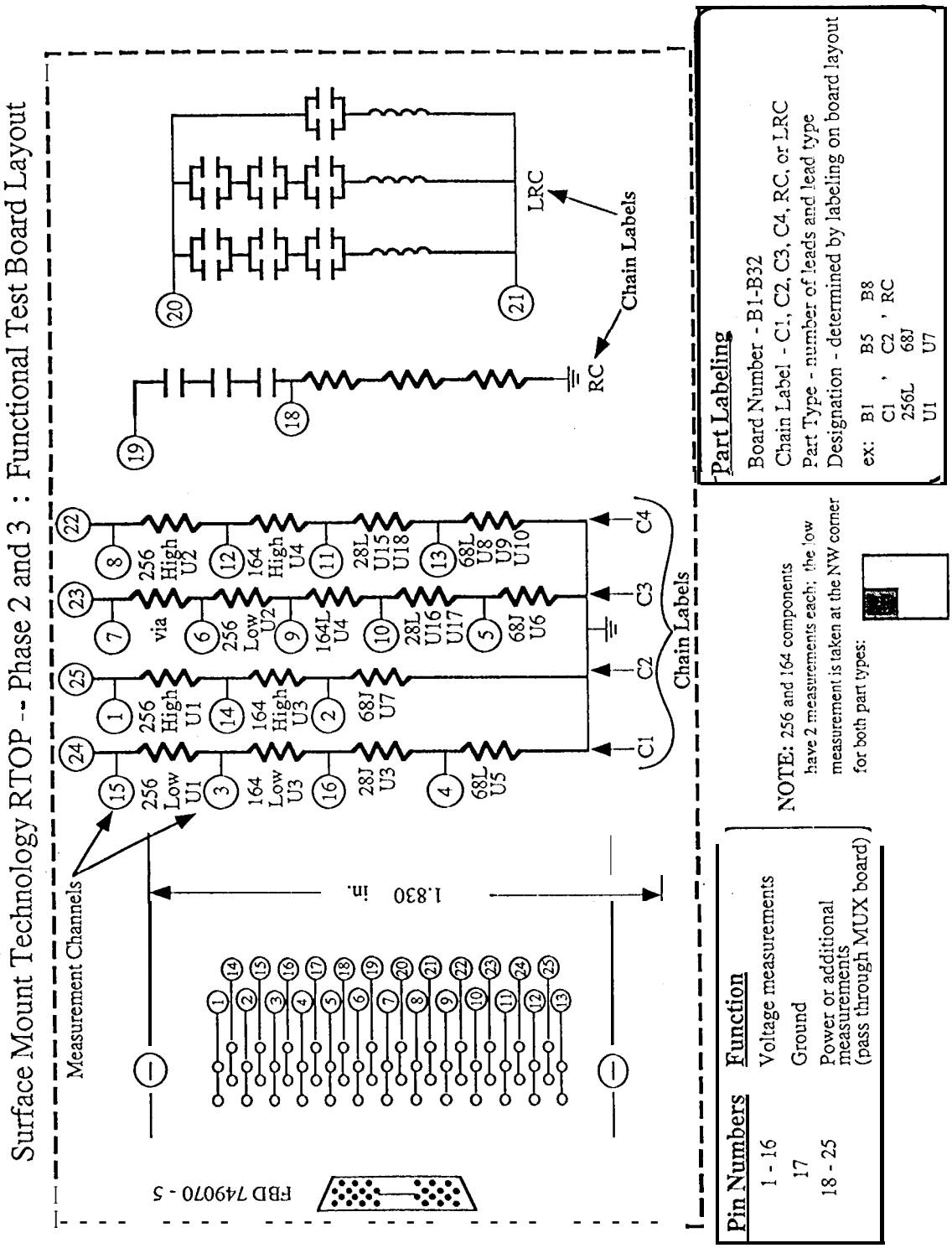

Figure 2 Functional layout of the test board

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NASA SMT HANDBOOK (NHB)

SMT Handbook Objective

The principal objective of the SMT NHB is to set forth surface mount technology for use at NASA installations within the context of concurrent engineering, To effectively utilize SMT as a packaging technology, this document sets forth both guidelines and appropriate requirements for the user. The emphasis throughout the handbook is on high reliability SMT assemblies that are produced in very small production lots. The requirements are established for two reasons:

- To ensure a more reliable product.
- To protect the environment.

To date, the Handbook is now approximately ninety percent (-90%) completed and has been extensively reviewed by knowledgeable industry members, both within NASA and outside,

SOLDER 1NTEGRIT%

Objectives

The objectives of the solder integrity investigation are as follows:

- Develop a thorough understanding of the creep-fatigue mechanisms underlying solder joint failures of important surface mount electronic packaging systems.
- Develop generic, broadly applicable design guidelines, analysis methodologies, and data required to achieve high reliability surface mount packaging by NASA centers and contractors.

The key emphasis of this RTOP effort is on differential expansion induced fatigue and creep of solder joints caused by part/board differential expansion and also expansion of conformal coating and part-bonding materials.

Research Activities

Solder integrity research activities are being conducted in five key areas:

1 Investigations to understand sensitivities to solder material properties and solder joint configurations due to differences in soldering processes (e.g., hand soldering versus mass reflow), storage aging, and grain growth.

2 Research in solder joint failure physics to assess the merits of different solder joint life prediction methodologies (SJLPMs). Special emphasis is placed on resolving inconsistencies found in the open literature, This is to be conducted through a joint effort between the SMT Solder Integrity RTOP and the Thermal Test Technology RTOP.

3 Extensive finite element creep-fatigue simulation modeling of important surface mount packaging systems to thoroughly quantify the parameter dependencies, design sensitivities, and relative life expectancies as a function of construction variables and applied stress levels.

4 Specialized thermal cycle experiments to confirm and augment the analytical predictions and to assist in understanding crack propagation and the metallurgical nature of cyclic damage at different stages.

5 Generation of guidelines addressing identified technical problems relevant to flight projects and related research activities. An important part of this activity involves understanding the complex interactions among crucial parameters such as the acceleration factors between qualification test environments and flight environments, failure detections, and statistical reliability assessments, The concurrent engineering approach of the other SMT RTOPS will be invaluable in understanding these interactions.

QUALITY ASSURANCE METHODOLOGY

The overall objectives of quality assurance (QA) investigations are to identify the critical manufacturing parameters and to determine methods and tools required to integrate QA procedures into the design and manufacturing process so that the critical parameters for ultralow volume applications may be bounded and controlled. The objective of the Phase 1 activities are:

- Identify and quantify the critical parameters of the methods and equipment currently used for SMT inspection and analysis in the commercial, military, and NASA.

- Evaluate alternative to manual, visual SMT inspection an analysis procedures and equipment. Identify their strengths and weaknesses, and adaptability of these methods and equipment to low production, high reliability SMT for space applications.

- Investigate in-process QA test and measurement techniques and methodologies applicable to ultralow volume SMT hardware.

- Identify critical parameters of commonly used SMT processes such as solder paste deposition, reflow, lead tin, etc. and then relate initial quality and reliability performance to the specific operations. Integrate significant finding into the NASA SMT Handbook.

- Provide recommendations for adaptation or development of equipment, tools methods and criteria for application to low manufacture SMT hardware design and manufacture.

- Integrate these activities with related JPL SMT efforts and other NASA center (Goddard, Marshall) efforts to provide mutual support and minimize duplication,

Extensive work has been done in meeting the objectives of QA activities. In this section our Phase 1 efforts on correlations between SMT manufacturing defects and part type, and inspection observation of thermal cycling degradation and the life of solder joints will be presented.

All Phase 1 assemblies were inspected prior to thermal cycling, and were continuously monitored for electrical solder joint failure and periodically inspected visually and by SEM as they are cycled to failure. Documentation of manufacturing defects, thermal damages, crack initiation and propagation will enable the creation of chronological damage maps, which will assist in the characterization of the severity of damages and the estimation of remaining solder joint life. Observations were documented for part type configurations, solder joint quality, lead materials and locations, and printed wiring board systems. Information obtained through these activities will be incorporated into design and reliability prediction guidelines, and training material for inspection and manufacturing personnel as well as revised NASA workmanship standards for SMT assemblies.

The defect codes used to document inspection observations and for entry into the Phase 1 database throughout the Phase 1 test arc given in the Table 1.

Table 1 DEFECT CODES: PHASE 1 INSPECTION

1 NO DEFECT (BEFORE CYCLING)	18 CRACK@ 50% FEATURE LENGTH
2 SOLDER BALLS/SPLASH	19 CRACK @ 75% FEATURE LENGTH
3 DEWETTING	20 CRACK @ 100% FEATURE LENGTH
4 NON-WETTING	21 SOLDER BRIDGE
5 INCLUSION	22 GRAINY SOLDER
6 VOID	23 LUMPY SOLDER
7 ICICLES/PROJECTIONS	24 STRETCH MARKS
8 INSUFFICIENT SOLDER	2S BOARD CONTAMINATION
9 EXCESS SOLDER	26 INSUFFICIENT TINNING
10 NO FILLET	27 LEAD SOLDERED TO BODY
11 LEAD OVERHANG	28 LEAD TOO HJGH
12 CONTAMINATION (ON SOLDER)	29 TOE DOWN
13 LIGHT STRESS	30 LEAD DEFORMED
14 MODERATE STRESS	31 DAMAGED SOLDER JOINT
1S HEAVY STRESS	32 CONTAMINATION (IN SOLDER)
16 POSSIBLE CRACK	99 NO STRESS DEFECT (AFTER CYCLING)
17 CRACK @ 25?6 FEATURE LENGTH	

Phase 1 Manufacturing Inspections

A summary graph of defects observed for part type during the manufacturing inspections prior to cycling appears in Figure 3. Defect types are those defined in the Table 1. As seen from Figure 3a, defects codes such as 4 (non-wetting), 7 (icicles), and 21 (solder bridging) are not included in the plot because they occurred less than one percentage. Inclusion (5), void (6), and light stress (13) defects were extremely small (near 1 %),

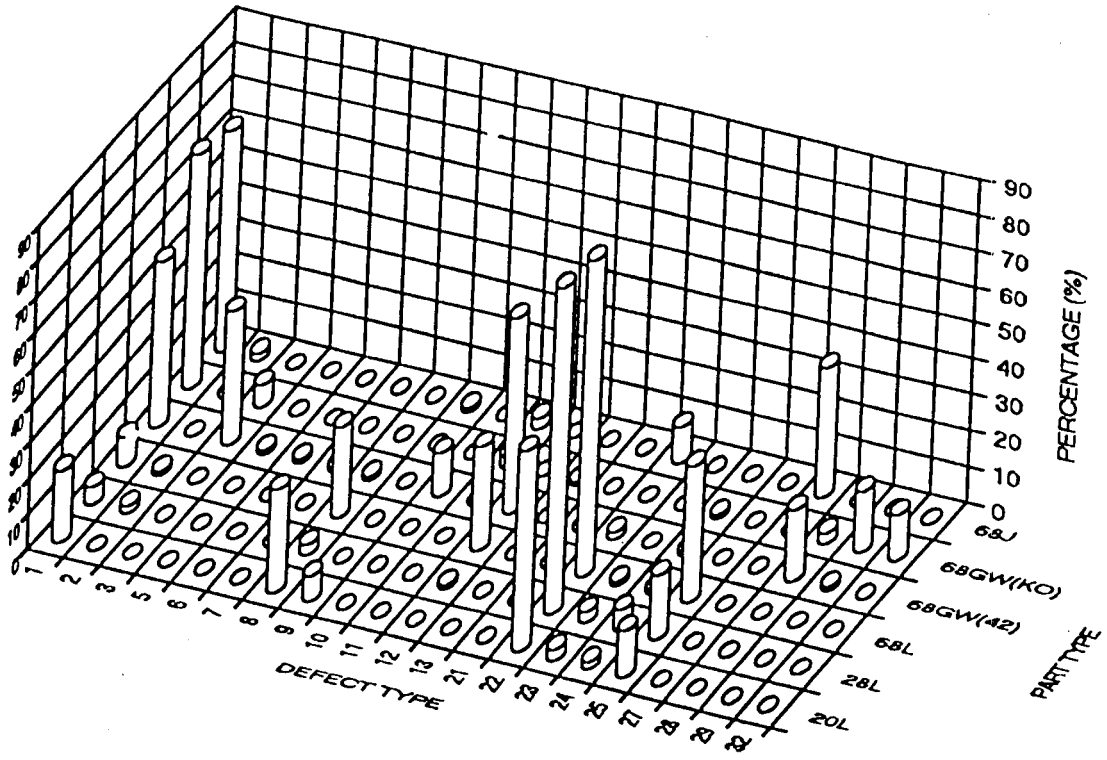
The next significant manufacturing defects were for those defects that are associated with the improper control of solder such as observation of excess (9) and lumpy (23) solder joints. Dewetting (3) and contaminations (12) of both solder and board were commonly occurred in most of the parts. Grainy (22) solder were frequently observed and the total percentage of this defect type was nearly equal to the total of other defects types.

These defects, irrespective of their importance in the solder joint life definition, were added to identify an indicator for the assessing the ease of solder joint manufacturability and potential life of leaded and leadless assemblies. The percentages of the solder defects for these assemblies are shown in Figure 3b. It is seen that manufacturing defects are much lower for the J-lead and gullwing leaded parts. Therefore a longer life and wider manufacturing process window for these types of assemblies is expected,

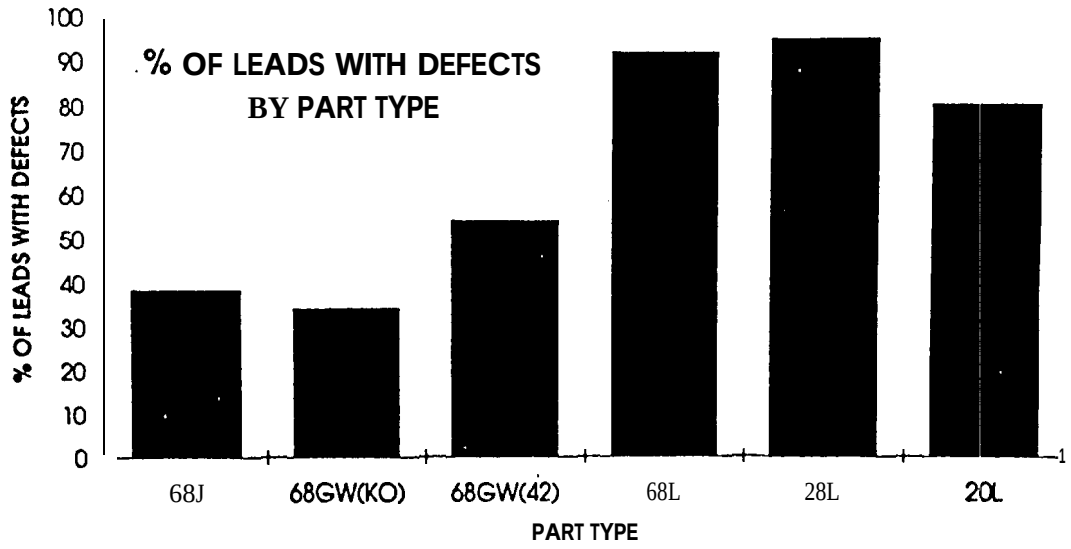
LCC Inspection Data Visualization

The Phase 1 thermal cycling test has yielded large quantities of inspection data, When viewed as raw data or as a data summary report of abstract numbers, it is often difficult to visualize what is actually occurring, and one tends to get "lost in the data." As part of this research and development effort, an innovative way of displaying inspection data has been developed allowing instant visualization of the data, especially the correlation with pin location on the inspected part. This method may be adapted for use with other types of data, and in conjunction with other graphical display methods, makes it easy to visualize complex data patterns.

Figure 4 through Figure 6 illustrate the use of this type of plot, The X and Y axes depict the pin location of the part. The Z (vertical) axis depicts a relative value assigned to various levels of stress, from 1 (no visible damage) through 9 (100% feature length crack). The X, Y, and Z axes arc nondimensional and show relative pin locations and stress indications. The examples shown below are typical for the part types and do not represent summary data or conclusions except for the specific serial numbers indicated.



a) Percentage of defects for part type



b) Percentage of total defects for part type

Figure 3 Manufacturing solder defects by part type (prior to cycling)

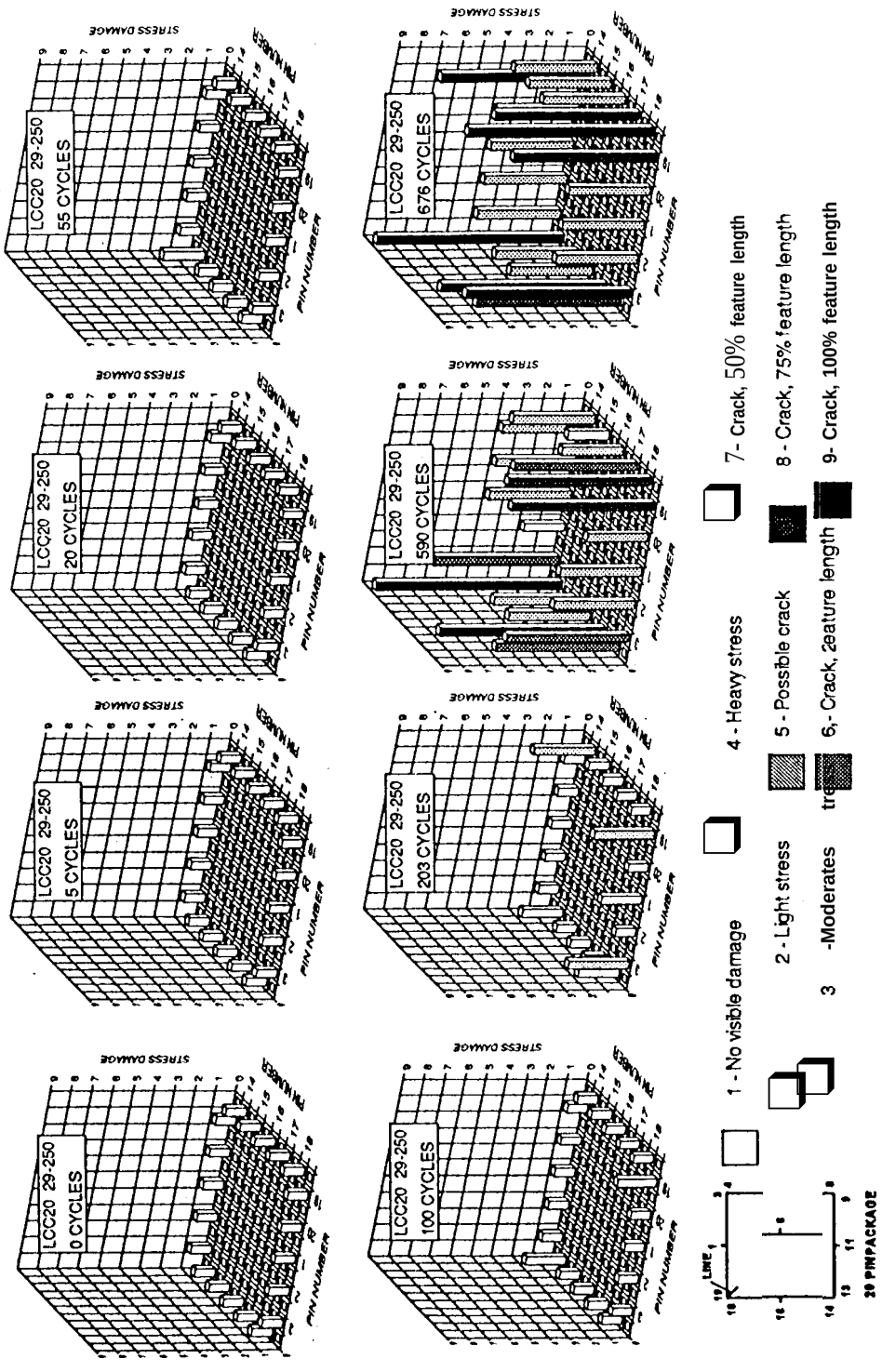


Figure 4 Visual indica ions of temp. cycle stress/cracks over time, LCC 20

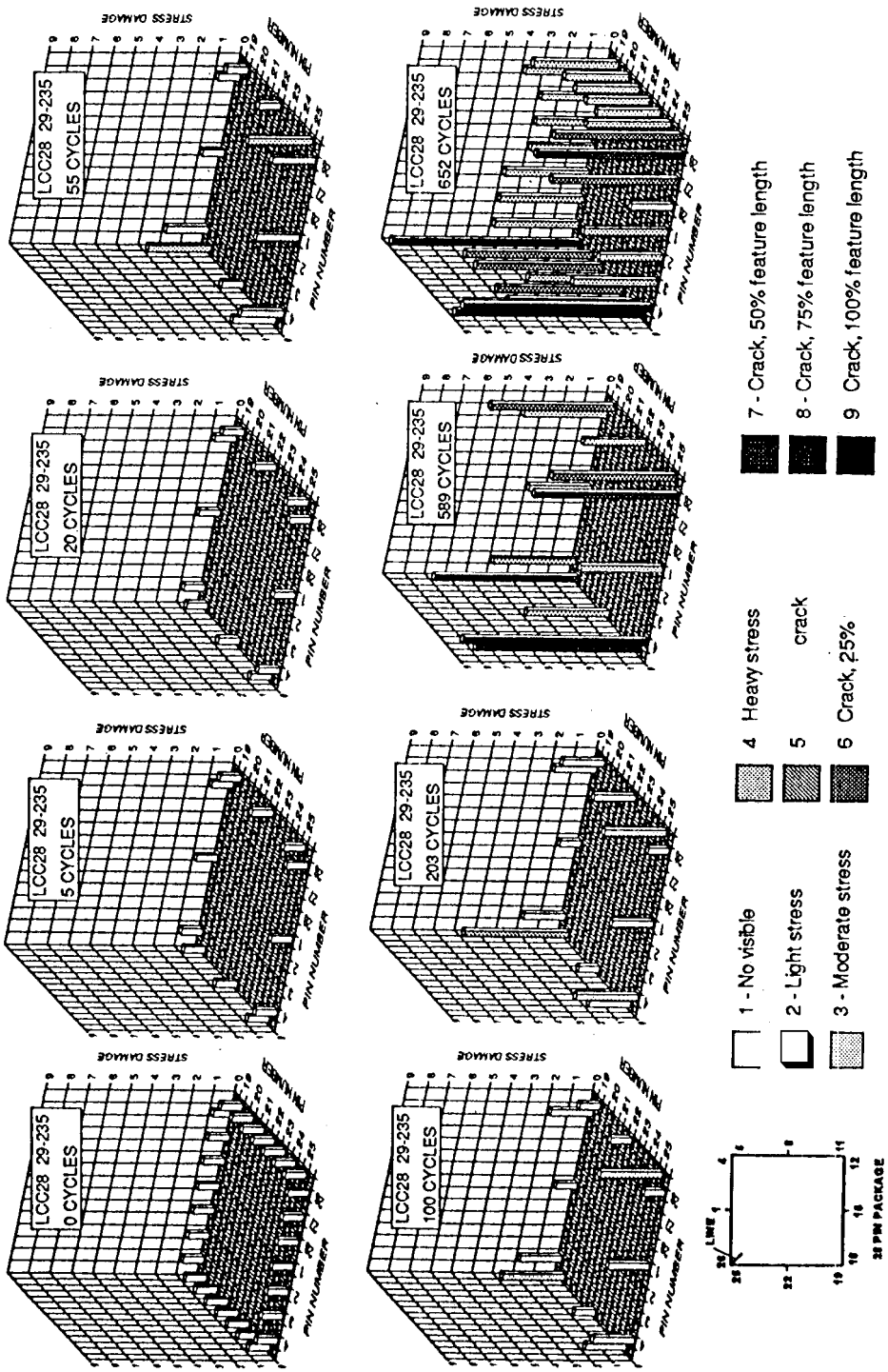


Figure 5 Visual indications of temp. cycle stress/cracks over time, LCC 28

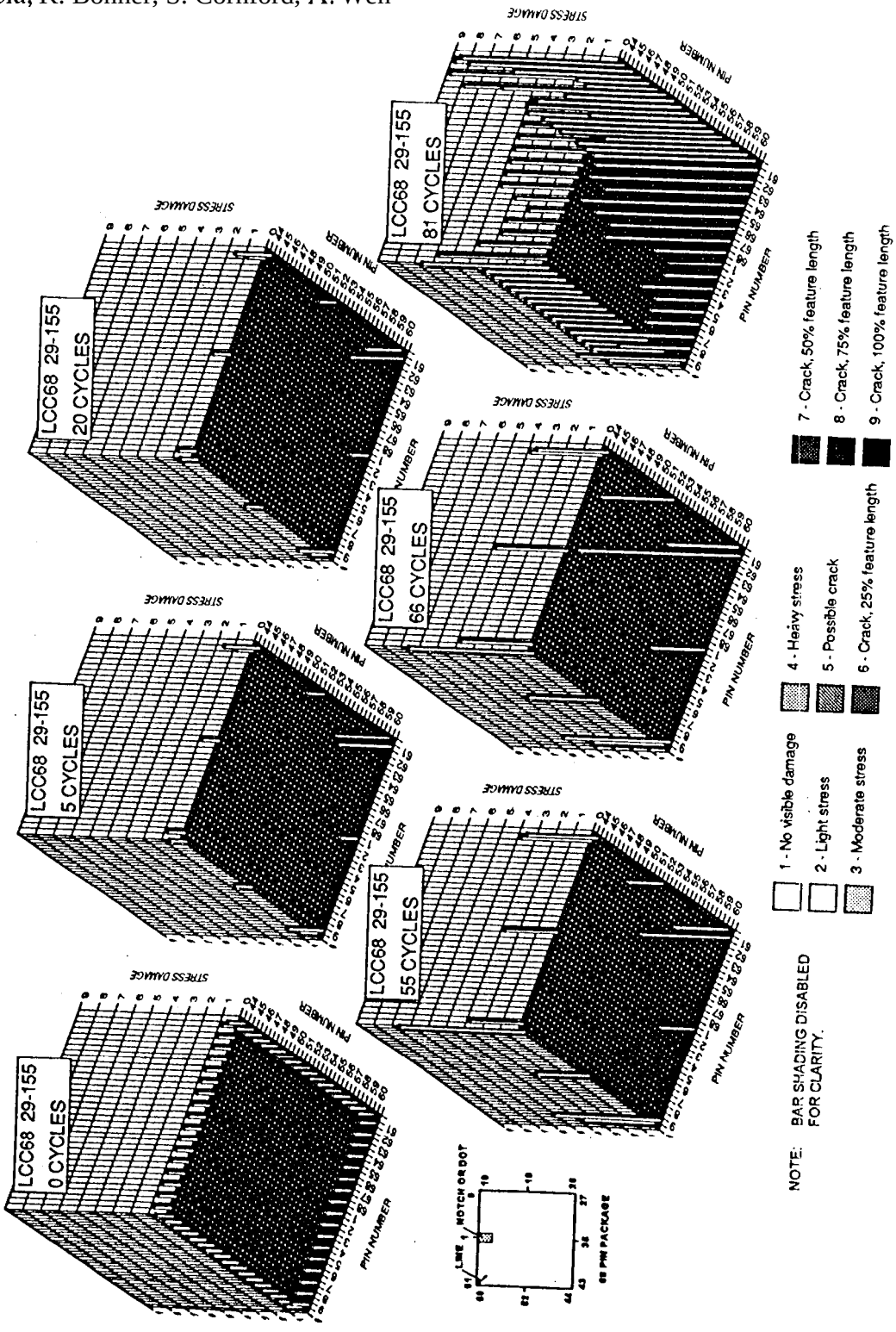


Figure 6 Visual indications of temp. cycle stress/cracks over time, LCC 68

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QUALIFICATION TEST TECHNOLOGY

Objectives

The long term objective of the Thermal Test Technology research and develpment effort is to develop NASA-wide assembly level qualification and acceptance test methodology for all packaging technologies being considered,

The objective and approach for the SMT Qualification portion of this research and development effort are:

- To develop and validate a qualification test methodology (exclusive of manufacturing flaws) for SMT packaged sub-assemblies.

Qualification Methodology Development

Based upon the results of an SMT survey, a methodology was developed to encompass the wide variety of NASA missions and of anticipated electronics packaging uses. This three-step methodology may be briefly summarized as:

1 Qualify the technology: identify the potential reliability and workmanship issues and appropriate screens, establish the limits of the technology by performing tests to failure on the particular packaging application and develop the appropriate procurement criteria,

2 Quantify the mission and the design: establish fatigue life/thermal cycling allocations and perform the appropriate reliability analyses necessary to ensure the application will meet the necessary reliability requirements.

3 Verify the design parameters: identify the key parameters for verification in the previously qualified hardware, determine the workmanship standards appropriate for the hardware and the means by which these are to be verified and perform the tests/screens to verify the analyses and quality,

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A methodology for the qualification of surface mount assemblies was developed earlier for use within this effort and inclusion in the NASA SMT NHB. It has been documented as JPL D-11469 available through the JPL Library Archive Center. laboratory. This methodology can be briefly summarized as follows:

- Qualify the technology application.
- Quantify the design and mission requirements.
- Verify the design parameters.

Another specific aspect of the qualification methodology which has been developed further is that of quantifying the means by which (1) a given set of test results (thermal profile, sample sizes, statistical failure distribution data, etc.) for a given piece of hardware may be used to assess the reliability (and risk) of the hardware in that mission application and (2) a qualification program may be designed to achieve a given level of reliability.

This approach utilizes the known failure distributions which occur during qualification testing. For example, different failure distribution shape parameters may result in different sample sizes and design/usage margins to achieve similar levels of reliability.

Open Issues

The primary open issues which need resolution are planned to be resolved during the testing program. They include:

1 The large discrepancy in the published data for solder fatigue,

This is being addressed in two different ways. First, the round-robin approach of the modeling efforts of the test vehicles will ensure that all of the various models are modeling the same test samples. This should eliminate the variabilities in the results due to purely experimental differences. Second, a joint study by L-C. Wen and S. L. Cornford is addressing the degree to which a modified Coffin-Manson equation can account for these discrepancies.

2 The means by which given mission thermal profile maybe translated into an equivalent (with appropriate margin) number of test cycles,

The test program will explore the dependencies of the failure distributions of the various package types on the thermal cycling environment. By performing the cycling of identical test vehicles over different temperature ranges, it is anticipated that a greater understanding of the effects of differences in the mean temperature and of the ranges will be better understood,

The goal of this portion of the test program is to develop acceleration factors for hardware cycled over different combinations of mission temperature cycles. It has been postulated (with some disagreement) that there are two different failure mechanisms at the high and low temperature extremes which combine during a standard NASA qualification test (-55°C to 100°C) to produce excessively conservative results. This temperature range dependence will also be investigated,

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